Foundations of On-chip Communication: Latency Issues in Multicore Platforms

Radu Marculescu
Carnegie Mellon University
Pittsburgh, PA 15213, USA

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Low-power Design. Computation vs. communication

Buffered wire

Pipelined wire

Network-on-chip

[D. Greenfield, S. Moore, Computer J., 2008]
Multicore platforms are large scale distributed systems at nanoscale; they are dominated by communication costs.

Last level cache (LLC)
Memory controller (MC) & channels
I/O controller(s)
QPI controller,
Power control unit (PCU), etc.

Need to understand the behavior of thousand core systems.
Network (routers+links) is the missing link in understanding.

[U. Ogras, Tutorial ASPLOS 2012]
This presentation focuses on the new CPS paradigm and its impact on future integrated systems.

**Structure**
- Architecture and small world effects

**Dynamics**
- Workloads and multiscale behavior

**Control**
- Power and resource management
Our first insight into communication-based design came through architecture (topology, buffer, etc.) optimization.
Can induce small-world effects in regular NoCs. This brings huge performance improvements

$b(n) = D(m,n) = m + n - 2$

$b(n) = D'(m,n) < m + n - 2$

$b(n) = \log_2 N$

This way, the fundamental idea of Small World networks (aka “six degrees of separation”) enters the multicore world
Flow-control mechanisms, reconfigurability, adaptive routing have all been used to improve performance.

7 One way or another, they all exploit the small world effects...
Small world effects can also be exploited to reduce hop count in 3D wireless NoCs and improve performance.

Wired and wireless NoCs can be used intra-chip, while inter-chip communication is based on wireless inductive-coupling.

[H. Matsutani et al. ASPDAC 2013]
Packet inter-arrival times at interface queues play a fundamental part in network behavior.
High injection rates cause inter-arrival times deviate from exponential distribution and exhibit power law correlations.

Workload analysis should not be an afterthought. In real platforms network traffic is neither Poisson, nor stationary.
Power management can be implemented via control-theoretic approaches in GALS designs.

Fine-grain power management becomes possible by exploiting workload variations.
Need a new paradigm shift, i.e., incorporate correlation structure of traces into dynamical state equations.

\[
\frac{d^{\alpha_s} x_k}{dt^{\alpha_s}} = G(x_k, f_j, f_l, t)
\]

Scale (Non-Fractal vs. Fractal) of Memory Effects in the Workload

\[
\min_{t_i}^{t_f} F(x_k, f_j, f_l, t)dt
\]

Fractal (State-Space) System Model

New Approaches (Constrained State & Control Variables Finite Horizon)

Fractal Optimal Control

Non-fractal (State-Space) System Model

Unconstrained State & Control Variables

Constrained State & Control Variables

\[
f_j^{\min} \leq f_j(t) \leq f_j^{\max}, \quad j = 1 + N_r
\]

Degree of Constraining State and Control variables

Scale (Finite vs. Infinite) of Time Constraints

Finite Time Horizon

Infinite Time Horizon

LQR, P, PI, PID
An hierarchy of globally distributed locally centralized control may help the system self-organize

- Orders of magnitude!
- Gets better with size

<table>
<thead>
<tr>
<th>System Size</th>
<th>Flat Mesh (nJ)</th>
<th>WiNoC (nJ)</th>
<th>Factor</th>
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</thead>
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<tr>
<td>128</td>
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<td>22.57</td>
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</tbody>
</table>

[Chang et al. IEEE Trans. Comp., 2010]

Local control w/ full state information, global control w/ partial information. Small world effects help convergence
Finally...

Contributors (in no particular order…)

Paul Bogdan (Univ. of Southern Calif.), Umit Y. Ogras (Intel/ASU), Partha Pande (Washington State Univ.), Diana Marculescu (Carnegie Mellon Univ), Qian Zhiliang (Hong Kong Univ Sci&Tech), Chi-Ying Tsui (Hong Kong Univ Sci&Tech), Hiroki Matsutani (Keio Univ).

Relevant papers - www.ece.cmu.edu/~sld

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